Attorney Docket: DA01028/1346P

10 Appeal Brief 12.23.02 C. Moore

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Grace Alicea

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of: Date: December 13, 2002

Mark S. CHANG, et al.

Serial No: 09/539,458 Group Art Unit: 2814

Filed: March 30, 2000 Examiner: Pham, H.

For: METHOD AND SYSTEM FOR PROVIDING CONTACT TO A FIRST POLYSILICON LAYER INA FLASH MEMORY DEVICE

Commissioner of Patents and Trademarks
Washington, D.C. 20231

APPEAL BRIEF TRANSMITTAL LETTER

Sir:

Submitted herewith are an original and two copies of Appellant's Brief on Appeal which is submitted under 37 C.F.R. 1.192 in connection with the above-identified Patent Application. The Brief includes and Appendix.

Please charge the Appeal Brief filing fee of $320.00 to Deposit Account Number 01-0365 (AMD, Inc.). A duplicate copy of this paper is attached.

Very truly yours,

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APPELLANT'S BRIEF

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APPELLANT'S BRIEF ON APPEAL

Sir:

Appellant herein files an Appeal Brief drafted in accordance with the provisions of 37 C.F.R. § 1.192(c) as follows:

I. REAL PARTY IN INTEREST

Appellant respectfully submits that the above-captioned application is assigned, in its entirety to Advanced Micro Devices of Sunnyvale, California.

II. RELATED APPEALS AND INTERFERENCES

Appellant states that, upon information and belief, he is not aware of any co-pending appeal or interference which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1, 2, 3, 4, 5, 6, and 7 are pending. Application Serial No. 08/714,915 (the instant application) as originally filed included claims 1-16. In a Response to a Restriction Requirement dated June 29, 2001, claims 1-7 were elected with traverse. In an Amendment dated December 19, 2001, claim 1 was amended to recite that the silicide layer resides on the first polysilicon layer but not between the plurality of floating gates and the plurality of control gates in the gate stack. In response to the Final Office Action, the Response dated August 20, 2002 did not amend any claims. Claims 1, 2, 3, 4, 5, 6, and 7 are on appeal and all applied prospective rejections concerning claims 1, 2, 3, 4, 5, 6, and 7 are herein being appealed.

IV. STATUS OF AMENDMENT

There was no proposed amendment in response to the Final Office Action.

V. SUMMARY OF THE INVENTION

The present invention provides an improved flash memory device including a plurality of gate stacks, at least one component, a silicide, an insulating layer, and a conductor. The gate stacks include a plurality of floating gates and a plurality of control gates. The component includes a polysilicon layer having a top surface on which the silicide resides. Although the silicide resides on the top surface of the component, the silicide does not reside between the floating gates and control gates of the gate stacks. The insulating layer covers the gate stacks, the component and the silicide. The insulating layer also has a plurality of contact holes therein. The contact holes are formed in an etch that uses the silicide as an etch stop layer so that the etch

does not etch through the polysilicon layer of the component. The conductor fills the contact holes so that electrical contact can be made to the underlying structure(s).

Figures 3B and 5B depict embodiments of the semiconductor devices 200 and 250 in accordance with the present invention. The silicide 228 and 274 resides on the components 226 and 272, respectively. In addition, contact holes 232, 234 and 236 and contact holes 280, 282 and 284 are depicted. As can be seen in Figures 3B and 5B, the contact holes 232, 234 and 236 and 280, 282 and 284, respectively, have different depths. Specification, page 9, line 9. In particular, the contact hole 234 to the source/drain region 206 is deeper than the contact hole 236 to the component 226. Similarly, the contact hole 282 to the source/drain region 256 is deeper than the contact hole 284 to the component 272. However, the contact holes 206 and 236 and the contact holes 256 and 284 are typically formed in the same step. Specification, page 8, line 4. In addition, some overetch may be performed in order to ensure that the contact holes 236 and 256 are at least the desired depths. Specification, page 9, lines 9-11. The silicide 226 and 272 can act as an etch stop. As a result, the underlying components 226 and 272 are not etched. Specification, page 9, lines 11-12 and page 13, lines 1-2. Consequently, the components 226 and 272 can still function.

VI. ISSUES

The issues presented are:

(1) whether claims 1, 2, 3, 4, 5, 6, and 7 are each unpatentable under 35 U.S.C. § 103 as being obvious in light of Applicant's Admitted Prior Art (AAPA) in view of U.S. Patent No. 5,065,220 (Patterson).

VII. GROUPING OF CLAIMS

Appellant hereby states that claims 1, 2, 3, 4, 5, 6, and 7 stand or fall together. Thus, claims 1, 2, 3, 4, 5, 6, and 7 are one group. Therefore, claims 1-7 constitute a single group.

VIII. ARGUMENTS

A. Summary of the Applied Rejections

In the Final Office Action, dated May 22, 2002, the Examiner rejected claims 1-7 under 35 U.S.C. § 103 as being unpatentable over Applicant's admitted prior art ("AAPA") in view of by U.S. Patent No. 5,065,220 ("Paterson"). In response to Applicant's arguments that if Paterson is added to the AAPA, the combination would still fail to teach or suggest that the silicide layer on the first component that resides on the first polysilicon layer does not reside between the plurality of floating gates and the plurality of control gates in the plurality of gate stacks, the Examiner stated that:

> [t]his argument is not persuasive since in the AAPA device, the silicide layer does not reside between the plurality of floating gates and the plurality of control gates in the plurality of gate stacks. The AAPA does not teach a silicide on the top surface of the polysilicon layer of the at least one component. However, Paterson et al. shows that is conventional in the art to have a device with a silicide (14) on [the] top surface of the polysilicon layer (12) as mention [sic] above.

Appellant respectfully requests that the Board reverse the Examiner's final rejection of claims 1, 2, 3, 4, 5, 6, and 7 under 35 U.S.C. § 103.

B. The Cited Prior Art

The AAPA describes semiconductor devices including gate stacks as well as other components. Such semiconductor devices are depicted in Figures 2A and 2B of the present application. The component 76 includes a first polysilicon (poly-1) layer. Specification, page 3

lines 7-8. Also depicted in AAPA are gate stacks which include a floating gate composed of a poly-1 layer and a control gate on the floating gate. Specification, page 3, lines 2-6 and Figure 1, items 60, 62 and 64. The component 76 depicted in the AAPA also includes an oxide-nitride-oxide (ONO) layer 78. Specification, page 4, lines 8-9. Thus, as the Examiner has acknowledged, the AAPA does not "teach a silicide on the top surface of the polysilicon layer of the at least one component, and the insulating layer etching step using the silicide as an etch stop layer to ensure that the insulating etching step does not etch through the polysilicon layer."

Figure 2B of the AAPA depicts the component after formation of the contact holes 82, 84 and 86. Specification, page 3, lines 14-15. The contact holes 82, 84 and 86 are formed concurrently. Specification, page 3, lines 17-18. The contact holes have very different depths. Specification, page 3, lines 14-15. Because the contact hole 86 to the component 76 is shallower than the contact hole 84, the component 76 has been etched through. Thus, the component 76 may be destroyed. Specification, page 4, lines 2-3. In addition, the underlying region, in this case the field oxide 54, may also be destroyed or damaged. Consequently, performance of the semiconductor device is adversely affected. Specification, page 4, lines 4-7.

Paterson describes a semiconductor that includes capacitors within a floating gate transistor. Paterson, Abstract, lines 1-3. A capacitor is typically composed of two plates (a lower plate and an upper plate) which are separated by an insulator. Paterson states that the capacitor has a "lower plate formed of polycrystalline silicon which, in this embodiment, is clad in a refractory metal silicide 14." Paterson, col. 2, lines 42-45. The capacitor also includes a top plate formed above the lower plate and silicide. Paterson, col. 2, lines 56-58. The silicide layer on the lower plate is provided "for additional stability of the capacitor 2." Paterson, col. 2, lines 49-50. The silicide layer thus resides between the bottom and top plates of the capacitor. Paterson, col.

2, lines 42-58 and Fig. 1. In addition to the capacitor, another structure having a top silicided surface (items 12, 14 of Fig. 1 of Paterson) is formed.

During formation of the capacitor, a first polysilicon layer is formed. The silicide is formed on the first polysilicon layer for all of the devices, including but not limited to the capacitor. Paterson, col. 3, lines 13-61. Although the silicide is used to enhance the voltage stability of the capacitor, the first polysilicon layer of all other structures is also silicided at the same. Paterson, col. 3, lines 54-61 and Figs. 2a-2h (silicide film 14 on layer 10 of the capacitor 2 as well as on item 12). Thus, both the capacitor (item 2 of Figs. 1 and 2a-2h) and the other structures (item 12) have a silicide film (item 14) on the first polysilicon layer (items 10, 12). Furthermore, Applicant can find no indication in Paterson that the silicide layer is removed on the capacitor or structures. Formation of the capacitor is completed by the formation of dielectric layers (silicon dioxide layer 20 and silicon nitride 22) and a conductive plate (metal layer 24) covering the dielectric layers. Paterson, col. 4, lines 14-17 and 39-42 and Fig. 1. Thus, Paterson teachings forming and keeping a silicide layer on the first polysilicon layer for all component. Stated differently, any silicide layer 14 residing the first polysilicon layer 12 of one component 12 is also on or within other components 2 that include the first polysilicon layer 10. See, for example, Fig. 1 of Paterson depicting the completed device and including silicide 14 between the plates 10 and 24 of the capacitor as well as on the polysilicon layer 12 of another component 12.

C. Claims 1-7 Are Not Unpatentable Under 35 U.S.C. § 103.

Appellant respectfully submits that the applied rejections of claim 1 under 35 U.S.C. § 103 are without merit as the Examiner has completely failed to explain why the AAPA in view

of Paterson teaches or suggests the methods recited in claim 1. With respect to claim 1, AAPA in view of Paterson neither teaches nor suggests:

> a silicide on the top surface of the polysilicon layer of the at least one component;
> [an] insulating layer having a plurality of contact holes therein, the plurality of contact holes being formed by etching the insulating layer to provide the plurality of contact holes, the insulating layer etching step using the silicide as an etch stop layer to ensure that the insulating etching step does not etch through the polysilicon layer; and . . .
> wherein the silicide layer resides on the first polysilicon layer but not between the plurality of floating gates and the plurality of control gates in the plurality of gate stacks.

In other words, AAPA in view of Paterson fails to teach or suggest using a silicide layer that resides on the top surface of the first polysilicon layer of a component, that acts as an etch stop layer to prevent etching of the underlying first polysilicon layer for the component, and that does not reside between the floating and control gates of the gate stacks.

As admitted by the Examiner in the Final Office Action, the AAPA fails to describe the use of a silicide layer that acts as an etch stop layer on the first polysilicon layer of the recited component. Instead, the AAPA teaches the use of a gate stack having a floating gate composed of a first polysilicon layer and a separate component that is also composed of the first polysilicon layer. Consequently, the AAPA alone does not teach or suggest the recited semiconductor devcie including the recited silicide layer.

Paterson fails to remedy the defect of AAPA. Paterson teaches that a silicide layer would be provided on the first polysilicon layer for **all** components in the semiconductor device. Thus, the first (lowest) polysilicon layer of Paterson is covered by a silicide layer. Paterson also teaches that this silicide layer remains on all the constituents of the semiconductor device (the capacitor and other device) that have a first polysilicon layer.

If the teachings of Paterson are added to those of the AAPA, the silicide layer of Paterson would be provided on the first polysilicon layer of **all** of the constituents of the semiconductor

device. This silicide layer would not be removed during fabrication. Consequently, if the teachings of Paterson are applied to the semiconductor device of AAPA, a silicide layer would be provided both on the floating gate 62 and on the polysilicon component 76 depicted in Figures 2A and 2B of the present application. Such a silicide layer would not be removed. Other layers, such as the ONO and control gate layers 64 and 66 depicted in Figure 2A of the specification, would be provided on this silicide layer when forming the gate stacks. Thus, this silicide layer would be present not only on the component 76 but also within other components such as the gate stacks and capacitors. This is contrary to the silicide layer recited in claim 1. As a result, even if the teachings of Paterson are added to those of the AAPA, the combination would still fail to teach or suggest the recited silicide layer that resides on the first polysilicon layer of the first component and that does not reside between the floating gates and the control gates in the gate stacks. The AAPA in view of Paterson, therefore, does not teach or suggest the flash memory device recited in claim 1. Accordingly, Applicant respectfully submits that claim 1 is allowable over the cited references.

Furthermore, Applicant respectfully disagrees with the Examiner's response to Applicant's arguments and respectfully submits that the Examiner's response to Applicant's arguments involves impermissible hindsight. It is well established that one "cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." In re Fine, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). See also In re Fritch, 23 USPQ2d 1780,1783 (Fed. Cir. 1992). In the response to Applicant's arguments, the Examiner appears to rely on Paterson's disclosure of the silicide layer on a component having a silicide top layer (item 12 of Fig. 1 of Paterson) to teach providing a silicide layer only on such a component. However, Paterson explicitly states that the silicide layer is provided on all of the components.

Furthermore, the silicide layer is provided for use within another component, the capacitor. The completed semiconductor device of Paterson also includes the silicide layer on all of the components on which the silicide layer was deposited. Applicant respectfully submits that the Examiner's use of Paterson to teach the silicide layer only on the additional component 12 without consideration of how and where Paterson forms the silicide layer (i.e. on all components and without removing the silicide layer on any components) involves impermissible hindsight. Consequently, Applicant respectfully submits that claim 1 is allowable over the cited references.

Claims 2, 3, 4, 5, 6, and 7 depend on independent claim 1. Consequently, claims 2-7 are allowable for the same reasons discussed above with respect to claim 1.

Accordingly Appellant respectfully requests that the Board reverse the final rejection of claims 1, 2 ,3, 4, 5, 6, and 7 under 35 U.S.C. § 103.

E. Summary of Arguments

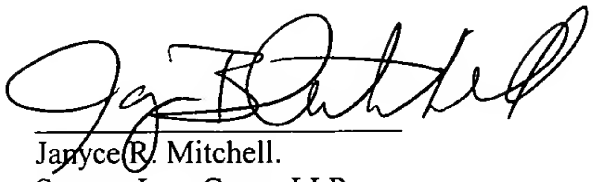
For all the foregoing reasons, it is respectfully submitted that Claims 1, 2, 3, 4, 5, 7, and 7 (all the claims presently in the application) are patentable for defining subject matter which would not have been obvious under 35 U.S.C. § 103 or anticipated under 35 U.S.C. § 102(e) at the time the subject matter was invented. Thus, Appellant respectfully requests that the Board reverse the rejection of all the appealed Claims and find each of these Claims allowable.

Note: For convenience of detachment without disturbing the integrity of the remainder of pages of this Appeal Brief, Appellant's "APPENDIX" section is contained on separate sheets following the signatory portion of this Appeal Brief.

This Brief is being submitted in triplicate, and authorization for payment of the required Brief fee is contained in the cover letter for this Brief. Please charge any fee that may be

necessary for the continued pendency of this application to Deposit Account No. 01-0365 (AMD, Inc.).

Very truly yours,



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IX. APPENDIX

1. (Amended) A flash memory device comprising:

a plurality of gate stacks including a plurality of floating gates and a plurality of control gates disposed on a semiconductor substrate;

at least one component including a polysilicon layer having a top surface;

a silicide on the top surface of the polysilicon layer of the at least one component;

an insulating layer covering the plurality of gate stacks, the at least one component and the silicide, the insulating layer having a plurality of contact holes therein, the plurality of contact holes being formed by etching the insulating layer to provide the plurality of contact holes, the insulating layer etching step using the silicide as an etch stop layer to ensure that the insulating etching step does not etch through the polysilicon layer; and

a conductor for filling the plurality of contact holes;

wherein the silicide layer resides on the first polysilicon layer but not between the plurality of floating gates and the plurality of control gates in the plurality of gate stacks.

2. The flash memory device of claim 1 wherein the silicide further includes a titanium silicide.

3. The flash memory device of claim 1 wherein the silicide further includes a cobalt silicide.

4. The flash memory device of claim 1 wherein the component further includes an oxide-nitride oxide layer on the polysilicon layer and wherein the oxide-nitride-oxide layer is removed prior to formation of the silicide.

5. The flash memory device of claim 4 wherein the oxide-nitride-oxide layer is removed during a second polysilicon layer etching step which forms the plurality of gate stacks.

6. The flash memory device of claim 4 wherein the plurality of gate stacks further include a plurality of spacers and wherein the oxide-nitride-oxide layer is removed after formation of the plurality of spacers.

7. The flash memory device of claim 1 further comprising:

at least one field oxide region, the at lest one component being located on the at least one field oxide region.